

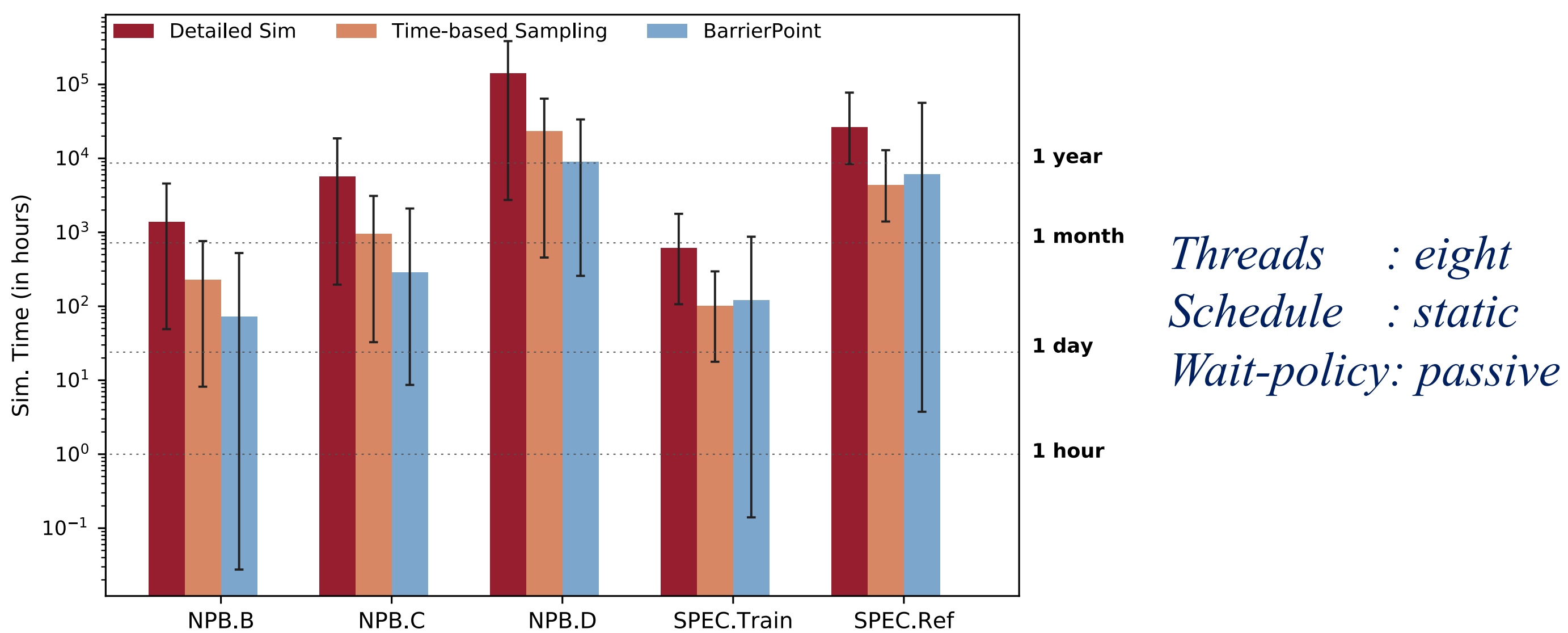
# Pac-Sim: Simulation of Multi-threaded Workloads using Intelligent, Live Sampling

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## 1. Introduction

- Microarchitecture simulation can take months to years
- Solution:** Sampled simulation



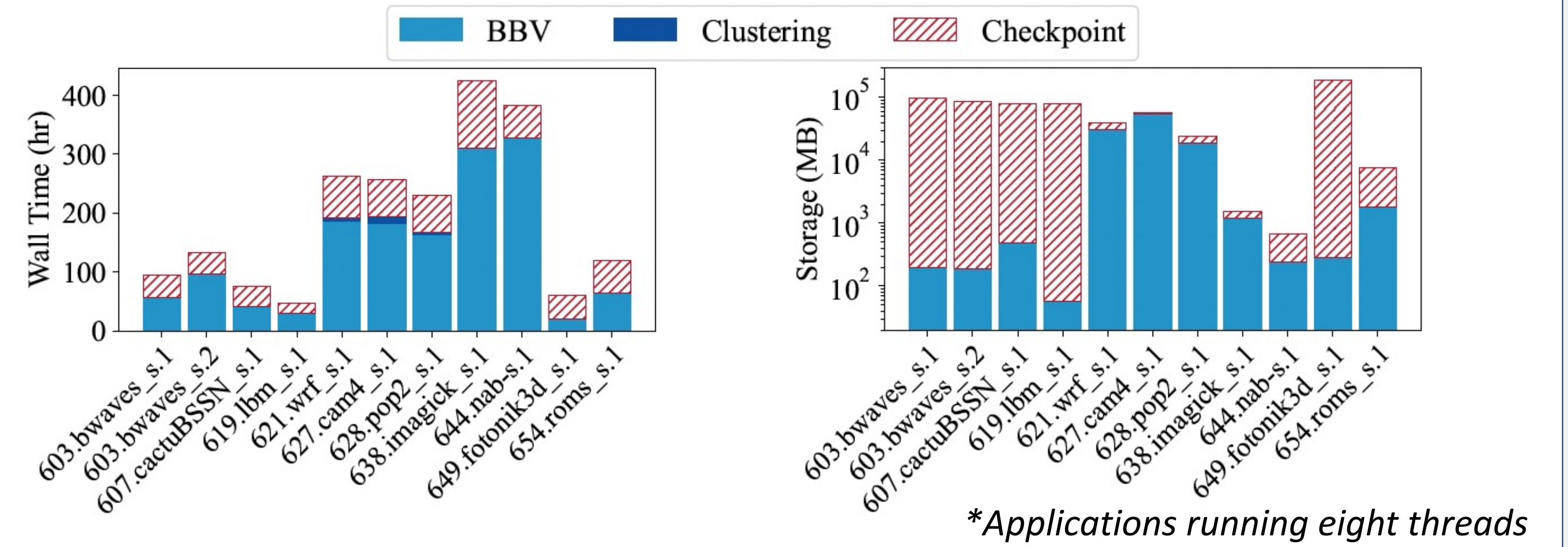
Drawbacks of prior multi-threaded sampling methodologies

Time-based Sampling	BarrierPoint, TaskPoint	LoopPoint
(i) Too slow; defeats the purpose	(ii) Application-specific techniques	(iii) Applies only to static workloads

We propose **Pac-Sim** to solve all these problems even in the presence of both hardware and software dynamism

## 2. Issues with Profile-Driven Techniques

### Overheads with LoopPoint Methodology\*



### Run-time Optimizations Invalidate Profiling Data

Hardware events

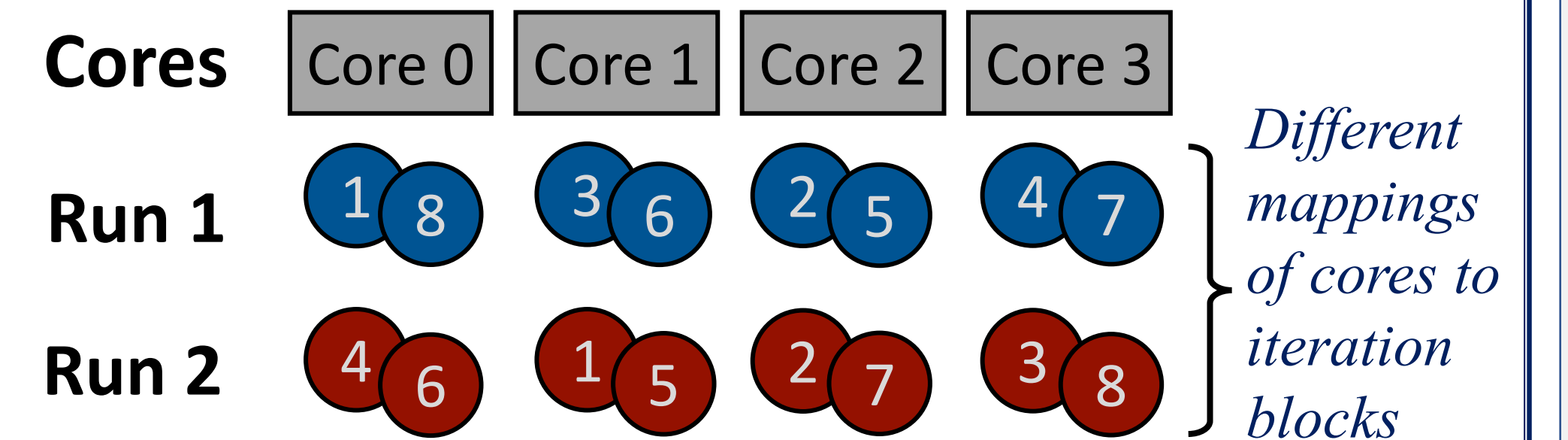
DVFS

Turbo Boost

Cache Reconfiguration

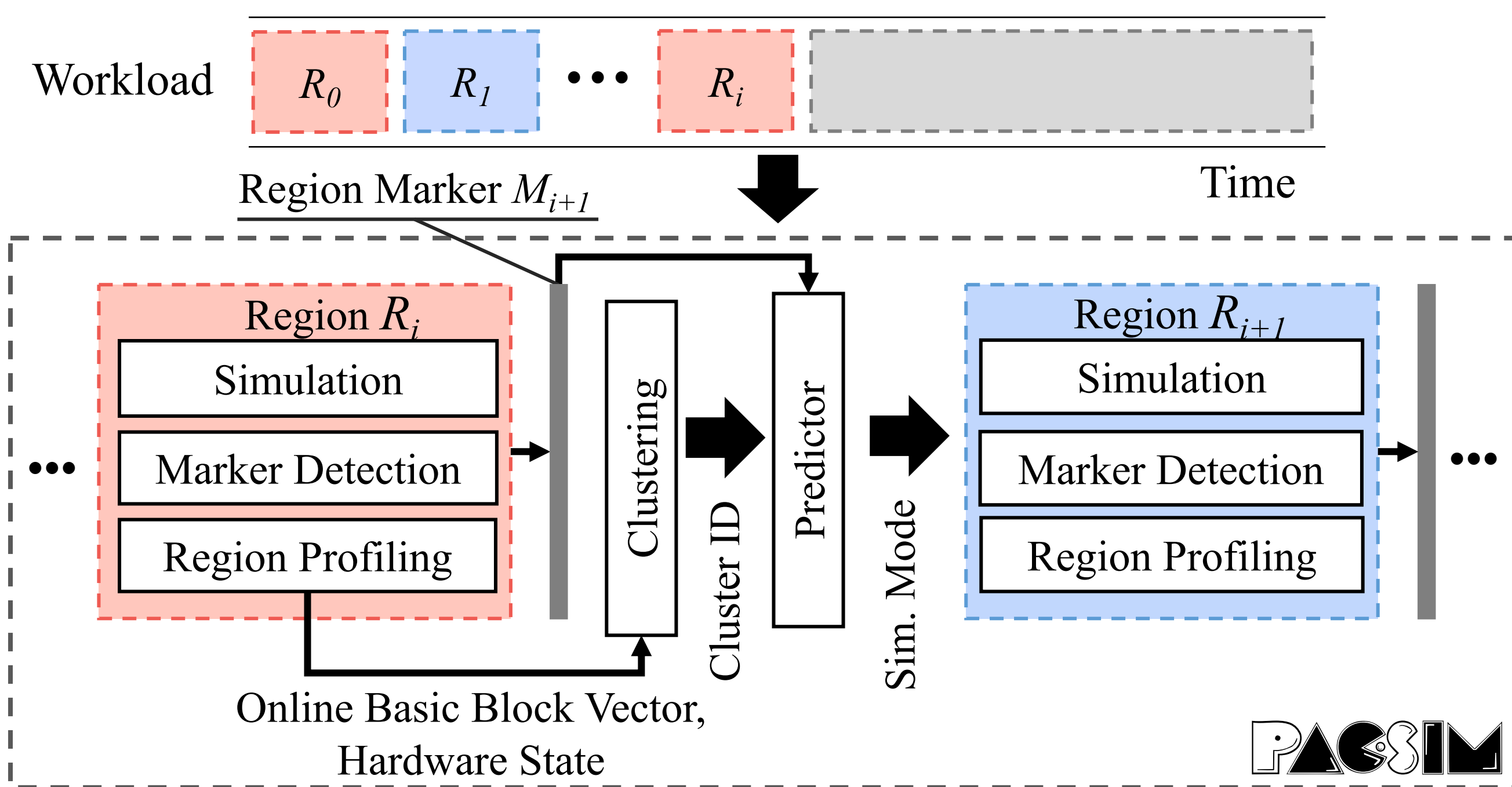
Dynamically scheduled threads

```
#pragma omp parallel for schedule(dynamic)
for(i=0; i<n; i++) {
    unpredictable_amount_of_work(i);
}
```



## 3. Pac-Sim Methodology

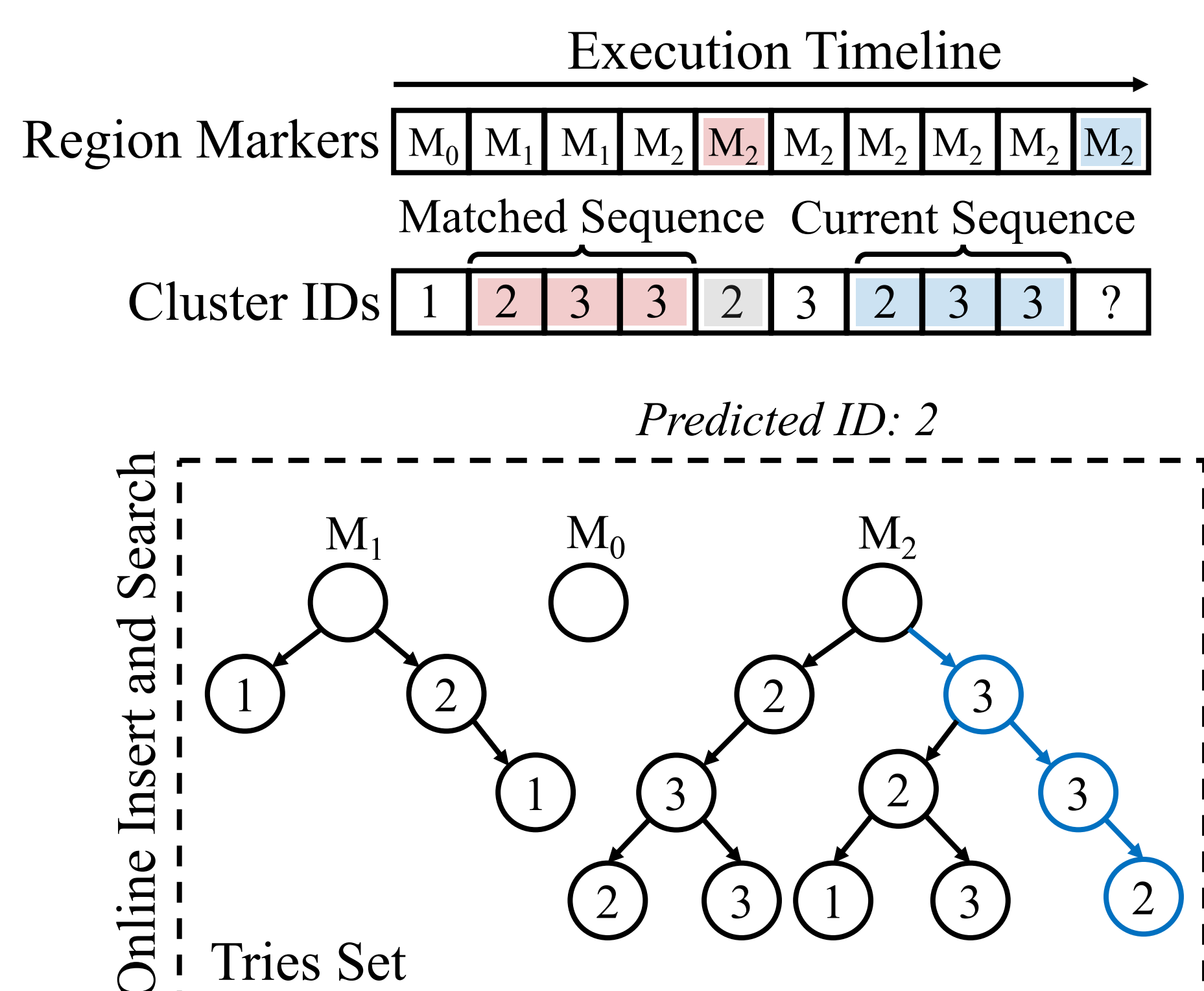
### 3.1 The Bigger Picture



- Determines simulation regions online which eliminates upfront profiling and checkpointing
- Marker Detection identifies the boundaries (as barriers or loops) of the current region
- Predictor determines if the next region is to be simulated in detail based on cluster info

### 3.2 Working of Predictor

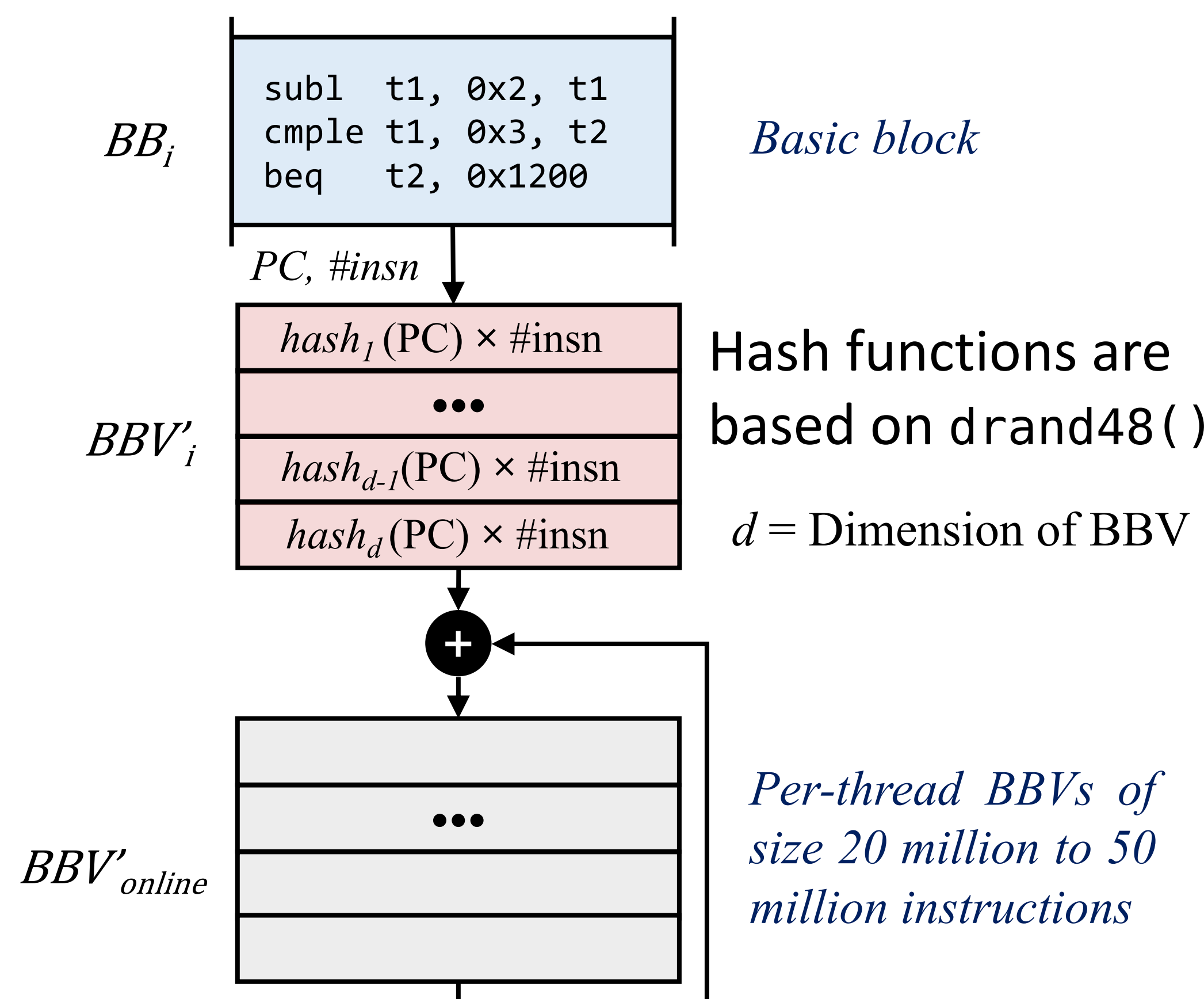
- Cluster history is stored using *tries*



- Next cluster is predicted from longest matching sequence of cluster history
- Pac-Sim uses tries with max-depth of 16

### 3.3 Online BBVs

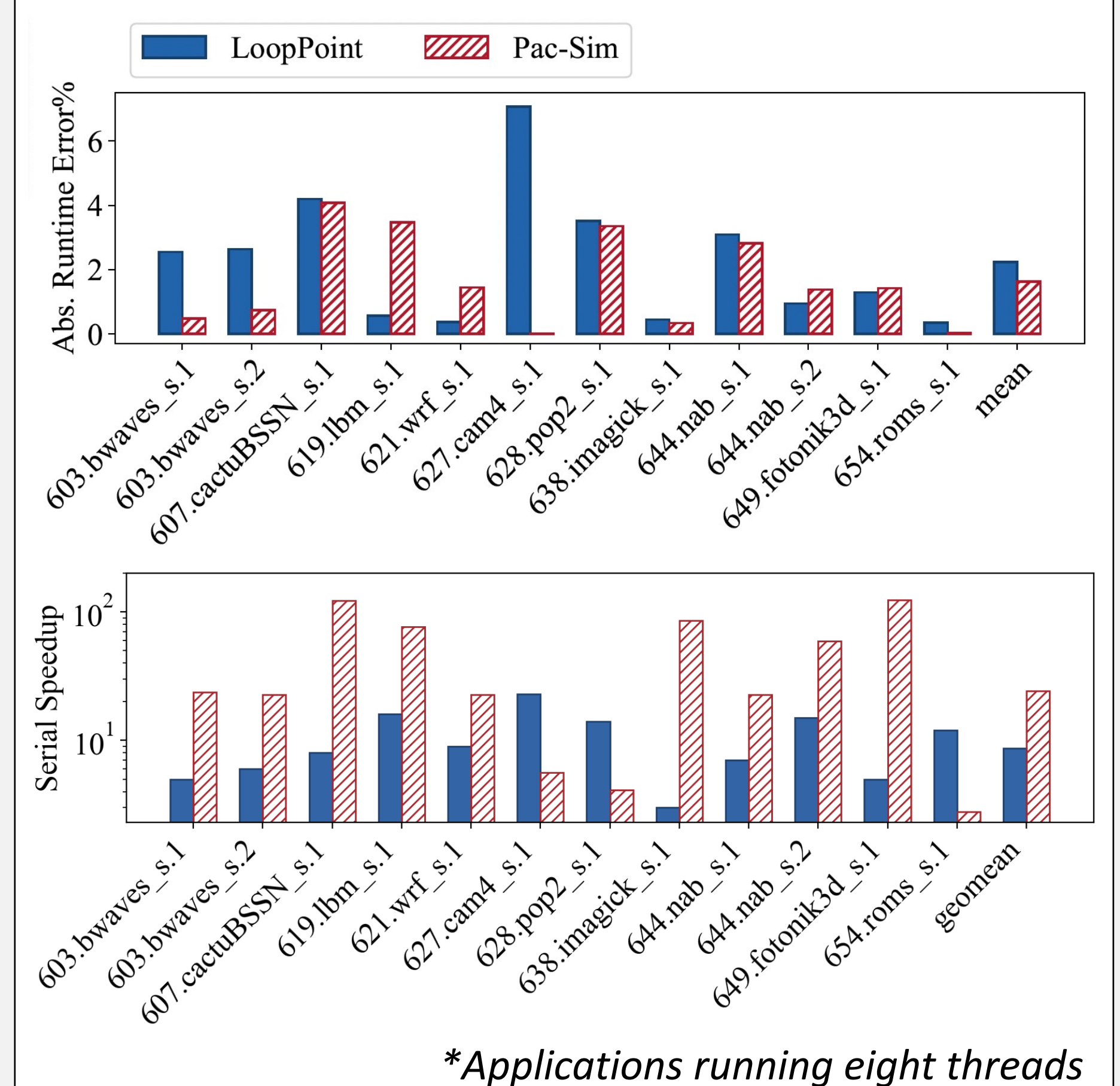
- Generated during the simulation of a region



$$BBV'_{online} = \sum_i BBV'_i = \sum_i (BBV_i \cdot Mproj)$$

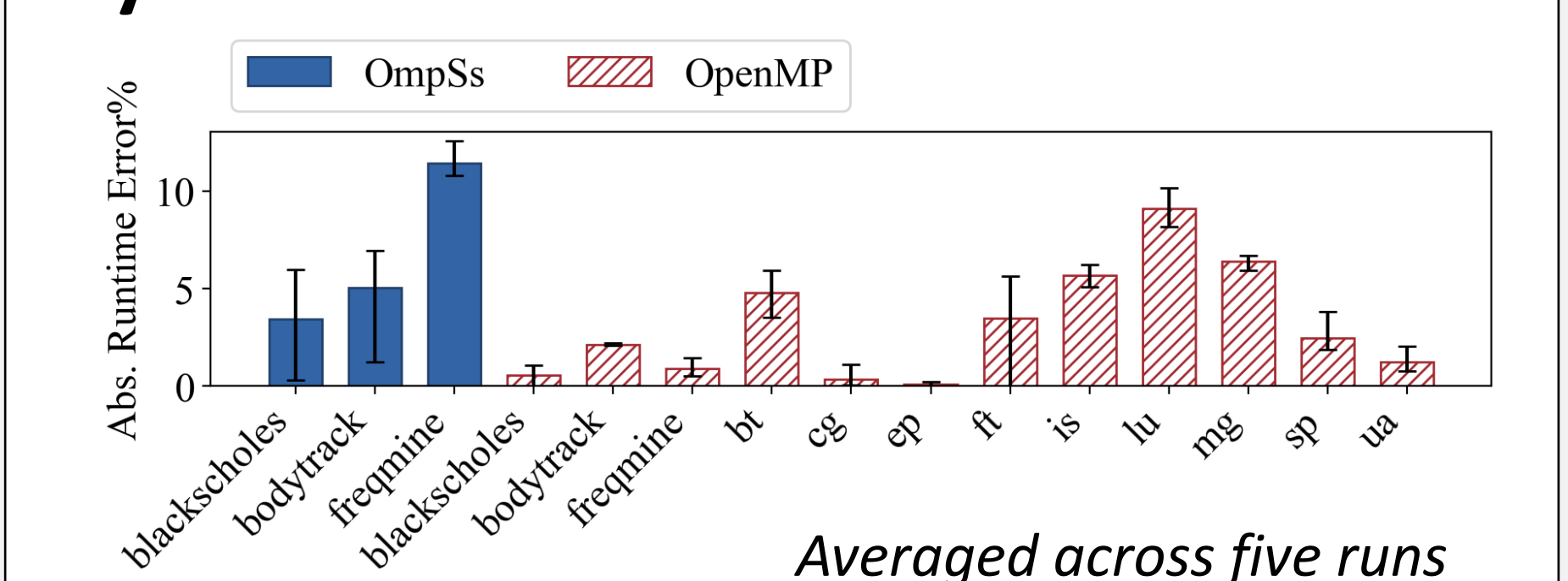
## 4. Experimental Results

### Accuracy and Speedup\*



## 5. Case Study

### Dynamic Software\*



### Dynamic Hardware\*

